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EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/511,575	PORST ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/26/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 are pending in this office action and presented for examination.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

a. In [0015], line 3, there appears to be a "t" typo.

b. Much of the specification appears to be grammatically and syntactically awkward, and it is difficult to follow the description of the invention or understand the crux of the invention. Any revisions that can be made without resulting in the addition of new matter to aid understandability would be appreciated by the examiner.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed by explicitly and concisely how the power-efficient control is achieved (e.g. by disabling idle functional units or so forth).

Double Patenting

4. Claims 1-3 of this application conflict with claims 11 and 12 of Application No. 10514850. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one

application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

5. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 12 of copending Application No. 10514850. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 12 of the '850 application contains all the elements of claim 1 of the instant application and thus anticipate the claim of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. Claims 2-3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 11 of copending Application No. 10514850 in view of Richter. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 2-3 of the instant application are obvious variants of claim 11 of the '850 application.

This is a provisional obviousness-type double patenting rejection.

7. Consider claims 2-3, this claim has additional limitations which are not taught by claim 11 of the '850 application, namely the limitations regarding the partial instruction words; however, each of these additional limitations are taught by Richter in the 103

rejection below. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Richter with the invention of the '850 application in order to achieve low power consumption (Richter, page 308, first paragraph under section B.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 recites the limitation:

c. "signal processors" in, for example, line 2, or "processors" in line 6; it is indefinite as to whether the limitation "signal processors" is used in the general sense, or whether the invention is directed toward a multiprocessing system with multiple signal processors.

d. "closed modules that are separate from one another" in lines 2-3; it is indefinite as to that makes a module "closed" and in what it means for a module to be separate from another as it could be logically separate (which itself is indefinite as to the scope), physically separate, and so forth.

e. "SIMD instructions" in line 5. There is insufficient antecedent basis for this limitation in the claim. Also, the acronym SIMD should be defined in the claims at its first mention similar to the other acronyms.

f. "SIMD instructions which are converted by a Processing Controlling Unit" in lines 5-6; it is indefinite as to what it means for SIMD instructions to be "converted."

g. "the processors" in line 6. There is insufficient antecedent basis for this limitation in the claim.

h. "a first and a second slice" in line 7; it is indefinite as to what a slice is or can be.

i. "the controlling effect" in line 9; it is indefinite as to what is trying to be conveyed.

j. "the controlling effect" in line 9. There is insufficient antecedent basis for this limitation in the claim.

k. "the single slice halt" in line 9; it is indefinite as to why this limitation is in quotation marks but the limitation in the previous line is not.

l. "being achieved by the bits" in lines 9-10; it is indefinite as to what is trying to be conveyed.

m. "the bits" in line 10. There is insufficient antecedent basis for this limitation in the claim.

n. "the bits, which are assigned to each slice," in line 10.; it is indefinite as to whether one or multiple bits are assigned to each slice.

o. "the register clock supply" in lines 10-11; there is insufficient antecedent basis for this limitation in the claim.

p. "the functioning" in line 12; there is insufficient antecedent basis for this limitation in the claim.

q. "the assigned input register" in line 12; there is insufficient antecedent basis for this limitation in the claim.

r. "the meantime" in line 13; there is insufficient antecedent basis for this limitation in the claim.

s. "the state" in line 13; there is insufficient antecedent basis for this limitation in the claim.

t. "enabling said functioning again" in line 15; it is indefinite as to how this is the case as the step in the claim is the first time in which the act of enabling is performed.

u. "SIMD instruction being converted" in line 16; it is indefinite as to what it means for an SIMD instruction to be "converted."

11. The overall syntax of claim 1 is also rejected as to being indefinite as the claim is unclear due to the current grammatical and syntactical structure; for example, the third paragraph which recites "by means...being achieved...switching..." and so forth.

12. Claim 2 recites the limitation:

v. "signal processors" in, for example, line 2, or "processors" in line 3, in addition to other places in the claim tree; it is indefinite as to whether the limitation "signal processors" is used in the general sense, or whether the

invention is directed toward a multiprocessing system with multiple signal processors.

w. "closed modules that are separate from one another" in lines 2-3; it is indefinite as to that makes a module "closed" and in what it means for a module to be separate from another as it could be logically separate (which itself is indefinite as to the scope), physically separate, and so forth.

x. "clock supply" in line 5; there is insufficient antecedent basis for this limitation in the claim.

y. "VLIW unit" in line 5; it is indefinite as to what exactly is a "VLIW unit."

z. "the state" in line 6; there is insufficient antecedent basis for this limitation in the claim.

aa. "the program flow" in line 6; there is insufficient antecedent basis for this limitation in the claim.

bb. "in such a manner" in line 6; it is indefinite as to what manner this is.

cc. "partial instruction words" in line 7; it is indefinite as to what a "partial instruction word" is.

dd. "the latter" in line 8; there is insufficient antecedent basis for this limitation in the claim.

ee. "the latter" in line 8; it is indefinite as to what "latter" is being referred to.

ff. "for multiple use at the functional units" in line 8; it is indefinite as to what is trying to be conveyed with this limitation.

gg. "the functional units" in line 8; there is insufficient antecedent basis for this limitation in the claim.

hh. The acronym VLIW should be defined in the claims at its first mention similar to the other acronyms.

13. Claim 3 recites the limitation:

ii. "the generation" in line 1; there is insufficient antecedent basis for this limitation in the claim.

jj. The acronym PCU should be defined in the claims at its first mention similar to the other acronyms as it is in a separate claim tree as independent claim 1.

kk. "this command" in line 3; it is indefinite as to which command is being referred to and should be explicitly recited.

ll. "the next clock cycle" in lines 3-4; it is indefinite as to the sequence of events, as it appears as claimed that the VLIW WAIT command is being applied to the PCU after the PCU has already been informed of a VLIW wait command and after generation of further VLIWs in the VLIW unit has occurred. In other words, it appears that the VLIW WAIT command is being applied to the PCU after the actions taken in response to receiving the VLIW WAIT command have already occurred.

mm. "the next clock cycle" in lines 3-4; there is insufficient antecedent basis for this limitation in the claim.

nn. "the clock supply" in line 4; there is insufficient antecedent basis for this limitation in the claim.

oo. "controlling the clock supply for a VLIW unit...in such a manner that, as a result, partial instruction words which are currently present in the VLIW unit are subsequently provided...."; it is indefinite as to how, if the VLIW unit (which is indefinite itself) is disabled, it can further provide those instructions to seemingly itself in tandem with future instructions.

14. Examiner would appreciate applicant's help in amending claims 2-3 to aid understandability, for example, by standardizing verb tenses and so forth.

15. Due to the extent of the indefiniteness of the claims, examiner has rejected the current claims with the prior art which appears to be closest to the subject matter at hand.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richter et al. (Richter) (A Platform-Based Highly Parallel Digital Signal Processor) in view of Gschwind et al. (Gschwind) (US 20030037221 A1).

18. Richter is cited in applicant's IDS paper filed 1/26/2005.

19. Consider claim 1, Richter discloses, as a result of the SIMD instructions which are converted by a Process Controlling Unit (PCU) of the signal processors, controlling parallel signal processing in the processors individually in data paths (DP) that are respectively associated with a first and a second slice (Figure 2, slices, PCU, data paths, DSP-core; page 307, left column, first unindented paragraph, SIMD approach). Richter also discloses of components such as registers (Figure 2), and thus inherently a register clock supply and gated clock cells (page 308, section B, bullet point 1, clock gating), an input register and accumulator (page 306, right column, section "Datapaths", a register file unit (Figure 2), and a memory access register (inherent given the load/store architecture; alternatively, the program counter).

However, Richter does not disclose the overall process of by means of a single slice halt state that is output by a Single Slice Mode (SSM) register bank, the controlling effect of the "single slice halt" state that has been output being achieved by the bits, which are assigned to each slice, of the SSM register bank, switching the register clock supply via respective first and second gated clock cells; as a result, stopping the functioning of the assigned input register and/or accumulator and/or pipeline control register in the meantime depending on the state of the signal processing occurring in the DP associated with the respective slice; and enabling said functioning again only when the single slice halt statethat has been output is discontinued as a result of a further SIMD instruction being converted, wherein a register file unit (RFU) and a memory access register of the processors remain in operation irrespective of the single

slice halt state that has been output and the PCU can in this case write to the SSM register bank of the PCU at any time.

On the other hand, Gschwind does disclose of a single slice halt state ([0042], selected functional units can be disabled) that is output by a Single Slice Mode (SSM) register bank ([0042], control logic 40 generates enable output signals; there must be some form of storage in the case of, for example, a last instruction executing, also see [0043], "on a subsequent operation" and not immediately after), the controlling effect of the "single slice halt" state that has been output being achieved by the bits (Figure 4, signals 402, which are bits), which are assigned to each slice (Figure 4, a signal to each functional unit), of the SSM register bank (the bits emanate from the control logic), switching the register clock supply via respective first and second gated clock cells ([0043] disable/enable the clock circuitry); as a result, stopping the functioning of the functional units ([0043], functional units will be disabled) in the meantime depending on the state of the signal processing occurring in the DP associated with the respective slice ([0042], selected functional units can be disabled); and enabling said functioning again only when the single slice halt state that has been output is discontinued as a result of a further SIMD instruction being converted ([0043], on a subsequent operation, the enabling output signals from control logic 400 will enable the clock circuitry), wherein a register file unit (RFU) and a memory access register of the processors remain in operation irrespective of the single slice halt state that has been output (the slice which is still be enabled will remain in operation even if another single slice is disabled) and the PCU can in this case write to the SSM register bank of the PCU at

any time ([0043], on a subsequent operation, the output signals can be enabled/disabled again).

The teaching of Gschwind enables the powering down of idle functional units which results in substantial system power savings (Gschwind, [0044]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gschwind with the invention of Richter in order to result in substantial system power savings. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the teaching of Gschwind would be able to be implemented into the environment of Richter; the functional units of Gschwind correlate to the slice-specific register files and MAC units of Richter. It would have been a readily recognized to one of ordinary skill in the art at the time of the invention that it would have been a design choice to use a register bank as storage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gschwind with the invention of Richter in order to result in substantial system power savings.

20. Consider claim 2, Richter discloses partial instruction words which are currently present in the VLIW unit are subsequently provided in the latter for multiple use at the functional units of the processors (page 305, first column, last paragraph, in this paper we present our M3-DSP; page 306, second column, section "Instruction Set Architecture", tagged VLIW, 32-bit wide instruction words in program memory are expanded by hardware to full VLIW width; the M3-DSP inherently has the specific

limitation; for a proof of inherency regarding tagged VLIW, see Lorenz et al, cited in the pertinent art, page 415, section 2, Target architecture M3-DSP, page 416, column 1, second to last paragraph, "A tagged VLIW method is used...[t]he idea is that the next VLIW is assembled by an instruction decoder for one or more TVLIWs which contain only functional unit instruction words for two function units; the number of required FIWs for assembling the next VLIW is *indicated by the IWC (instruction word class)*"; thus, for this to occur, partial instruction words which do not meet the number of required FIWs must be subsequently provided to future FIWs fetched later on so that all may be simultaneously executed at the functional units).

However, Richter does not disclose controlling the clock supply for a VLIW unit of the processors by means of a software- dictated output of the state from the program flow of the processors.

On the other hand, Gschwind does disclose controlling the clock supply for a VLIW unit of the processors by means of a software- dictated output of the state from the program flow of the processors ([0042], selected functional units can be disabled by disabling the clock input; it would have been readily recognized in the case of all no-op instructions, all unit would be shut down).

The teaching of Gschwind enables the powering down of idle functional units which results in substantial system power savings (Gschwind, [0044]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gschwind with the invention of Richter in order to result in substantial system power savings.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gschwind with the invention of Richter in order to result in substantial system power savings.

21. Consider claim 3, Richter and Gschwind discloses the generation of further VLIWs in the VLIW unit is interrupted by a PCU of the processors being informed of a VLIW WAIT command via an advance signal line and wherein this command is applied to the PCU in the next clock cycle (the current amount of FIWs, when below the instruction word class, must inherently notify a VLIW word forming unit to not form a VLIW word out of those FIWs until more FIWs arrive; this notification is the command and it is inherent a command is delivered via some sort of signal line), the PCU then switching the clock supply for the VLIW unit by means of a VLIW WAIT signal line and a third gated clock cell of the processors (Gschwind as disclosed above; it would have been readily recognized to one of ordinary skill in the art at the time of the invention that Gschwind's control logic can be implemented or combined with the PCU of Richter such that it is logically the PCU "block" which disables the clock signals of the functional units)..

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

pp. Brooks et al. (Dynamically Exploiting Narrow Width Operands to Improve Processor Power and Performance) discloses of dynamically shutting down functional units for instructions such as a parallel add instruction with narrow width operands. As a parallel add instruction is a type of SIMD instruction, this disclosure is particularly relevant to applicant's invention.

qq. Lorenz et al. (Optimized Address Assignment for DSPs with SIMD Memory Accesses) is used as proof of inherency regarding the features of a specific DSP in claim 2 above.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

kv

RICHARD L. ELLIS
PRIMARY EXAMINER